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PATENT APPLICATION  
2207/11269

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: FLETCHER, Thomas

Application No.: 10/020,447

Group Art Unit: 2121

Examiner: Not assigned

Filed: December 18, 2001

For: LOOK-AHEAD CARRY ADDER CIRCUIT

INFORMATION DISCLOSURE STATEMENT

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Technology Center 2100

Director of the U.S. Patent and Trademark Office  
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Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The paragraphs marked below are applicable.

- 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date or the date of filing a CPA, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.
- 2. This Information Disclosure Statement is being filed with a Request for Continued Examination (RCE). No certification or fee is required.
- 3. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.
- a. I hereby certify that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

- b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).
- c. Please debit Deposit Account No. 11-0600 in the amount of \$240.00 in payment of the fee under 37 CFR §1.17(p) to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached.
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Respectfully submitted,

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**INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

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Sheet

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of

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**Complete if Known**

Application Number	10/020,447
Filing Date	December 18, 2001
First Named Inventor	FLETCHER, Thomas
Group Art Unit	2121
Examiner Name	Not assigned
Attorney Docket Number	2207/11269

**U.S. PATENT DOCUMENTS**

Examiner Initials *	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
		6,208,907 B1	03/27/2002	DURHAM et al	

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				

**OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		Yee et al, "Clock-Delayed Domino for Dynamic Circuit Design", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 4, August 2000, pp 425-430	
		Yee et al, "Clock-Delayed Domino for Adder and Combinational Logic Design", IEEE, 1063-6404/96, pp 332-337, 1996	
		Jung, Perepelitsa, Sobelman, "Time Borrowing in High-Speed Functional Units Using Skew-Tolerant Domino Circuits," Proceedings, IEEE International Symposium on Circuits and Systems, pp. V-641 - V-644, 2000	
		Presentation by Carl Sechen dated March 17, 2000.	RECEIVED
		Taub, <i>Digital Circuits and Microprocessors</i> , pages 205-212, Mc-Graw-Hill, 1982	MAR 05 2002

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Examiner Signature	Date Considered
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